REMARKS

Claim Rejections - 35 USC §103 and New Matter Rejections

The Examiner summarizes the criteria for determining obviousness under 35 USC 103(a) based on the considerations established in Graham v. John Deere Company, 383 US 1, 148 USPQ 459 (1966) and applied admitted prior art (figures 1A-1C and Specification, prior art discussion, pages 1-7, hereinafter "APA") in view of Wang et al. (USPN 5,629,237, hereinafter "Wang").

It is respectfully submitted that amended claims 1 and 11 now meet all four Graham v. John Deere Company factors to show the nonobviousness of Applicant's claims as explained in the Applicant's Response of December 12, 2001, which is incorporated herein by reference thereto. Essentially, with regard to:

1. Determining the scope and contents of the prior art: The scope and contents of APA disclose a rectangular channel intersecting with a cylinder with no particular relationship and Wang discloses a tapered via with no channel.

2. Ascertaining the differences between the prior art and the claims at issue: The admitted prior art and Wang do not teach or suggest a collimator structure between the channel opening and the via opening.

3. Resolving the level of ordinary skill in the pertinent art: Those of ordinary skill in the pertinent art would be those skilled in the semiconductor device manufacturing art who have been unable to solve the problem solved by the Applicant's claimed invention as indicated in APA cited in Specification page 3, lines 21-25 (statement replicated below).

4. Considering the objective evidence present in the application indicating obviousness or nonobviousness: APA indicates that a solution to uniform formation of seed layers in vias has long eluded those skilled in the art and thus that the Applicant's claimed invention is unobvious.

Therefore, it is respectfully submitted that Applicant's claimed invention is unobvious under Graham v. John Deere Company.

The Examiner rejected claims 1-20 under 35 USC §103(a) as being unpatentable over APA in view of Wang.

The independent claims 1 and 11 have now been clarified to amend the previously claimed combination, as exemplified in claim 1, to now include the limitation that:

> "a dielectric layer formed over said semiconductor substrate and said semiconductor device, said dielectric layer having a channel opening and a via provided therein; said via having a via entrant angle formed from a rim of said channel opening to a rim of the via and a horizontal bottom of the channel opening of greater than about 69 degrees whereby said channel opening forms a collimator for said via and a depth and a cross-sectional area of the channel opening are determined by the via entrant angle" [underlining added for clarity]

The above amendment is not new matter for the "angle formed" and "collimator" of the above amendment since this matter is supported on Specification page 7, lines 21-25:

> "In the present invention, the second channel opening 103 is configured so that its width at the rims 134 form the via entrant angle 69 with the rim 132 of the via opening 105. This causes the rims 134 to act as a collimator for subsequent plasma or ion deposition processes where the deposition of the second adhesion/barrier layer 138 requires this "channel collimator effect"."

The above amendment is not new matter for the "cross-sectional area" of the above amendment since this matter is supported on Specification page 8, lines 12-16:

> "As would be evident to those skilled in the art, the via entrant angles are a function of the channel depth, and the cross-sectional area of the second channel 107 would still be sufficient to accommodate any current flow required through the via 109. Further, the current carrying capacity of the second channel 107 can be increased by making it deeper, which would also increase the channel collimation effect."

The above clarifies that there is a specific relationship between the via and the channel opening; i.e., the rim of the channel and the rim of the via. Basically, the specific relationship is such that the depth of the channel and its cross-sectional area are defined in the Applicant's claimed invention.

Neither APA nor Wang, singularly or in combination, teaches or suggests the above relationship where the structure of the via is related to the depth and cross-sectional area of the channel.

APA states in Specification page 3, lines 21-25:

> "A solution, which would form uniform seed layers in vias and result in an improvement in the subsequent filling of the vias by conductive materials, has long been sought, but has eluded those skilled in the art. As the semiconductor industry moves from aluminum to copper and other types of high conductivity materials, it is becoming more pressing that a solution be found."

Thus, at the time of APA, there was teaching or suggestion of any relationship between the via and the channel, which would provide uniform seed layers in the vias.

Wang is a method for forming a tapered contact via hole (Wang Abstract) and there is no teaching or suggestion of a channel.

It is respectfully submitted that the Federal Circuit recently vacated a judgment of the Board of Patent Appeal and Interferences in *In re* Sang-Su Lee, No. 00-1158 (Fed. Cir. Jan.18, 2002) where the Board had held that "the conclusion of obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference." The Federal Circuit held that a showing of a suggestion, teaching, or motivation to combine prior art references is an essential component of an obviousness holding. The Court emphasized that this need for specificity pervades precedential authority and that teachings of references can be combined only if there is some suggestion or incentive to do so.

Laitram Corp. v. Cambridge Wire Cloth Co., 226 USPQ 298, cited in the Applicant's Response of December 12, 2001, is one of the precedents.

It is believed that the now amended claims 1 and 11, and the claims depending therefrom, are now unobvious over APA in view of Wang, taken either singularly or in combination, under 35 USC 103(a).

The dependent claims 2-10 and 12-20 respectively depend from independent claims 1 and 11, and are believed to be allowable since they contain all the limitations set forth in the independent claims from which they depend and claim non-obvious combinations thereof.

Conclusion

In view of the above, it is submitted that the claims are in condition for allowance and reconsideration of the rejections is respectfully requested. Allowance of claims 1-20 at an early date is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including any extension of time fees, to Deposit Account No. 01-0365 and please credit any excess fees to such deposit account.

Respectfully submitted,

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NOTE: The "VERSION WITH MARKINGS TO SHOW CHANGES MADE" begins on the following page.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

- Please amend claims 1 and 11 by inserting the underlined text and deleting strike-through text as follows:

1. (Amended) An integrated circuit chip comprising:

a semiconductor substrate;

a semiconductor device over said semiconductor substrate;

a dielectric layer formed over said semiconductor substrate and said semiconductor device, said dielectric layer having a channel opening and a via provided therein~~;~~, said via having a via entrant angle formed ~~with~~ from a rim of said channel opening to a rim of the via and a horizontal bottom of the channel opening of greater than about 69 degrees whereby said channel opening forms a collimator for said via and a depth and a cross-sectional area of the channel opening are determined by the via entrant angle;

a seed layer lining said channel opening and said via; and

a conductive layer damascened into said seed layer and said dielectric layer whereby said conductive layer in said channel opening is operatively connected by said conductive layer in said via to said semiconductor device without voids.

11. (Amended) An integrated circuit chip comprising:

a semiconductor substrate;

a semiconductor device on said semiconductor substrate;

a first channel dielectric layer formed over said semiconductor substrate and said semiconductor device, said first channel dielectric layer having a first channel opening provided therein;

a first seed layer lining said first channel opening in said first channel dielectric layer;

a first conductive layer damascened into said first seed layer and said first channel dielectric layer whereby said conductive layer in said first channel opening is operatively connected to said semiconductor device;

second channel and via dielectric layers formed over said first channel dielectric layer, said second channel and via dielectric layers having a second channel opening and a via provided therein~~;~~, said via having a via entrant angle formed ~~with~~

from a rim of said second channel opening to a rim of the via and a horizontal bottom of the channel opening of greater than about 69 degrees whereby said second channel opening forms a collimator for said via and a depth and a cross-sectional area of the second channel opening are determined by the via entrant angle;

a second seed layer lining said second channel opening and said via; and

a second conductive layer damascened into said second seed layer and said second channel dielectric and via layers whereby said second conductive layer in said second channel opening is connected by said second conductive layer in said via to said first conductive layer in said first channel without voids.